A Monolithic GaAs 1–13-GHz Traveling-Wave Amplifier

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Abstract—**This paper describes a monolithic GaAs traveling-wave amplifier with 9-dB gain and ±1-dB gain flatness in the 1–13-GHz frequency range. The circuit is realized in monolithic form on a 0.1-mm GaAs substrate with 50-Ω input and output lines. In this approach, GaAs FET's periodically load input and output microstrip lines and provide the coupling between them with proper phase through their transconductance. Experimental results and the circuit details of such a structure are discussed. Initial results of a noise analysis and predictions on the noise performance are also given.**

I. Introduction

THE POTENTIAL of traveling-wave or distributed amplification for obtaining gains over wide frequency bands has long been recognized. There is a vast amount of literature on the subject and therefore only two representative references are given [1], [2]. In this approach, the input and output capacitances of electron tubes or transistors are combined with inductors to form two lumped-element artificial transmission lines. These artificial transmission lines are coupled by the transconductance of the active devices.

In actual circuits, however, the extreme bandwidths predicted by a first-order theory are modified by several factors, such as capacitive and inductive couplings, loading of the lumped-element transmission lines due to grid and coil losses, lead inductance, and parasitic capacitances associated with the coil windings. In circuits which employ FET's as the active elements, the gate and drain loading plays a very significant role in the operation and the high-frequency performance of the amplifier.

A new approach to traveling-wave amplification, which is more suitable for obtaining wide-band gain at microwave frequencies, was reported earlier [3]–[5]. In this approach, GaAs FET's are used as the active elements, and the input and output lines are periodically loaded microstrip transmission lines. With such an arrangement, the factors mentioned above as degrading the expected performance are either completely eliminated or their effect is included in the design.

II. Amplifier Design Considerations

A simplified equivalent-circuit diagram of the amplifier is shown in Fig. 1. In this circuit, microstrip lines are periodically loaded with the complex gate and drain impedances of the FET's, forming lossy transmission line structures of different characteristic impedance and propagation constant. The resultant effective input and output propagation structures are referred to as the gate and drain lines.

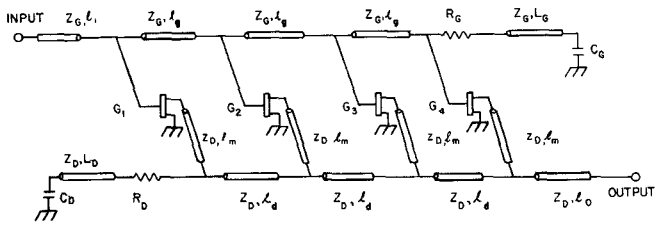

Fig. 1. Schematic representation of four-stage FET traveling-wave amplifier.

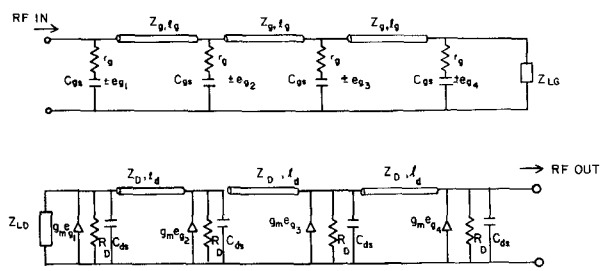

Fig. 2. Simplified equivalent-circuit diagram of FET traveling-wave amplifier.

An RF signal applied at the input end of the gate line travels down the line to the other end, where it is absorbed by the terminating impedance. However, a significant portion of the signal is dissipated by the gate circuits of the individual FET's along the way. The input signal sampled by the gate circuits at different phases (and generally at different amplitudes) is transferred to the drain line through the transconductance of the FET's. If the phase velocity of the signal at the drain line is identical to the phase velocity of the gate line, then the signals on the drain line add. The addition will be in phase only for the forward-traveling signal. This can readily be verified by examining the various possible signal paths between the input and output terminals. Any signal which travels backward, and is not quite cancelled by the out-of-phase additions, will be absorbed by the complex drain impedance.

A simplified equivalent-circuit diagram for the amplifier is shown in Fig. 2. In conventional amplifiers, one cannot increase the gain-bandwidth product by paralleling FET's, because the resulting increase in transductance g_m is compensated for by the corresponding increase in the input and output capacitances. The distributed amplifier over-

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comes this difficulty by adding the individual g_m's of the FET's without adding their input and output capacitances. If the spacing between the FET's is small compared with the wavelength, the characteristic impedances of the gate and drain lines shown in Fig. 2 can be approximated as

$$Z_g \simeq \left[L_g/(C_g + C_{gs}/l_g)\right]^{1/2} \tag{1}$$

and

$$Z_d \simeq \left[L_d/(C_d + C_{ds}/l_d)\right]^{1/2} \tag{2}$$

where L_g, C_g and L_d, C_d are the per-unit-length inductance and capacitance of the gate and drain lines, respectively. C_{gs} is the input gate-to-source capacitance and C_{ds} is the output drain-to-source capacitance of the unit cell FET; l_g and l_d are the lengths of the unit gate- and drain-line sections, respectively (see Fig. 2). The effect of resistive components r_g and r_d are neglected. The impedance expressions in (1) and (2) are clearly independent of the number of FET's used in the circuit.

Using the simplified equivalent-circuit of Fig. 2 and approximating the gate and drain lines as continuous structures, the gain expression for an n-cell circuit can be derived as

$$G = g_m^2 Z_d Z_g \left| \frac{\gamma_g l_g \left[\exp(-\gamma_g l_g n) - \exp(-\gamma_d l_d n)\right]}{\gamma_g^2 l_g^2 - \gamma_d^2 l_d^2} \right|^2 \tag{3}$$

where

$$Z_g \simeq \left[\frac{L_g}{C_g + \dfrac{C_{gs}}{l_g}} \right]^{1/2}$$

$$Z_d \simeq \left[\frac{L_d}{C_d + \dfrac{C_{ds}}{l_d}} \right]^{1/2}$$

and

$$\gamma_g \simeq j\omega \sqrt{L_g \left(C_g + \frac{C_{sg}}{l_g} \right)} + \frac{1}{2} \frac{r_g \omega^2 C_{sg}^2}{l_g} \sqrt{\frac{L_g}{\left(C_g + \dfrac{C_{sg}}{l_g} \right)}} \equiv j\beta_g + \alpha_g$$

$$\gamma_d \simeq j\omega \sqrt{L_d \left(C_d + \frac{C_{ds}}{l_g} \right)} + \frac{1}{2} \frac{1}{R_D l_d} \sqrt{\frac{L_d}{\left(C_d + \dfrac{C_{ds}}{l_d} \right)}} \equiv j\beta_d + \alpha_d.$$

Under normal operating conditions, the signals in the gate and drain lines are near synchronism ($\beta_g l_g \simeq \beta_d l_d$). If it is further assumed that $|\gamma_g| \simeq |\beta_g|$, and $|\gamma_d| \simeq |\beta_d|$, and $Z_g \simeq Z_d \equiv Z_0$, (3) can be simplified to

$$G = \frac{g_m^2 Z_0^2}{4} \frac{\left[\exp(-\alpha_g l_g n) - \exp(-\alpha_d l_d n)\right]^2}{(\alpha_g l_g - \alpha_d l_d)^2}. \tag{4}$$

This expression clearly shows that, as the number of cells n is increased, gain does not increase monotonically. This conclusion is in contrast to early tube distributed amplifier theories. In fact, as n gets large, gain approaches zero in the limit.

For values of $\alpha_g l_g n \leq 1$ and when drain-line losses are neglected compared with gate-line losses, (4) can be rewritten as

$$G \simeq \frac{g_m^2 n^2 Z_0^2}{4} \left(1 - \frac{\alpha_g l_g n}{2} + \frac{\alpha_g^2 l_g^2 n^2}{6} \right)^2. \tag{5}$$

We note that, in this operating regime, gain can be made proportional to n^2.

The gain expression derived above represents the actual circuit response reasonably well and can be used as a useful design tool. For instance, if a practical upper limit for the gate-line attenuation is assumed as $\alpha_g l_g n \leq 1$, then using the expression for the gate-line attenuation constant α_g, we find

$$r_g \omega^2 C_{sg}^2 Z_0 n \leq 2. \tag{6}$$

Thus we observe that, for a given FET, the maximum number of cells n that can be employed in the traveling amplifier can be determined from (6). Since the gate periphery of a unit cell is known, (6) also brings an upper limit to the total gate periphery that can be used in a practical amplifier. Clearly, this upper limit should be determined at the high end of the frequency band where satisfying the inequality of (6) is most difficult.

The performance of the traveling-wave amplifier was examined in a 2–12-GHz design band as a function of the more significant FET parameters such as r_g and R_D and the number of cells n. For this study, the simplified equivalent circuit of a FET traveling-wave amplifier shown in Fig. 2 was used and typical 1-μm gate length GaAs FET parameters assumed.

In Fig. 3, gain is plotted as a function of frequency as the number of cells or sections is varied. Clearly there is an optimum for n; going above that optimum value actually degrades the gain, starting from the high frequency end of the design band where gate and drain loading is the most severe.

In Fig. 4, the effect of the gate loading is examined as the gate resistance r_g used in the design (22 Ω) is set to zero or doubled. One can redesign the circuit elements to regain the flat gain performance, as shown in Fig. 5. This figure clearly indicates that the resistive part of the gate loading typically results in 3-dB gain reduction and doubling the effect of this loading gives an additional 3-dB reduction in gain. However, it is satisfying to see that the gain response can still be flattened despite assumed large attenuation on the gate line.

RF voltage variation along the gate line at individual

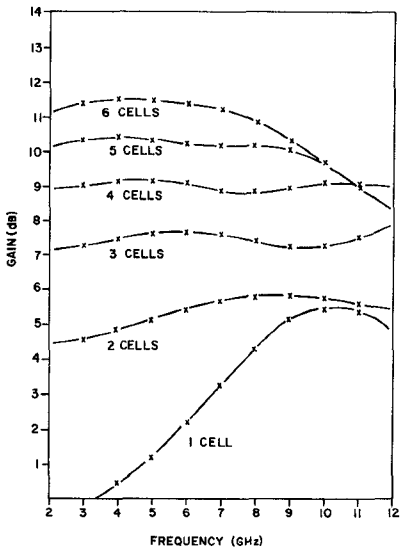

Fig. 3. Gain versus frequency, as the number of cells is varied.

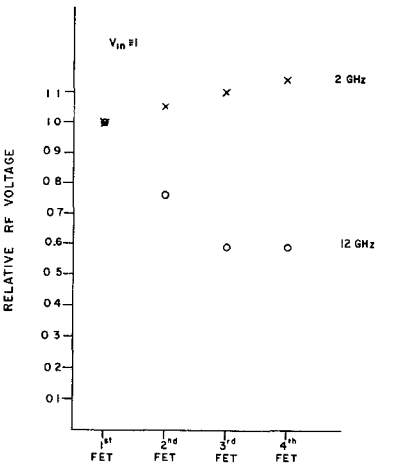

Fig. 6. Variation of the microwave signal along the gate line, at actual gate positions.

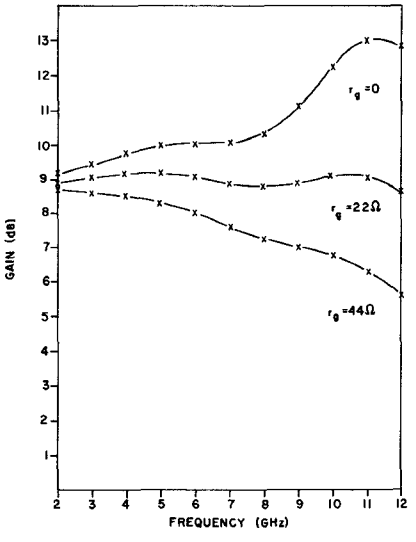

Fig. 4. Effect of the gate loading on gain versus frequency response.

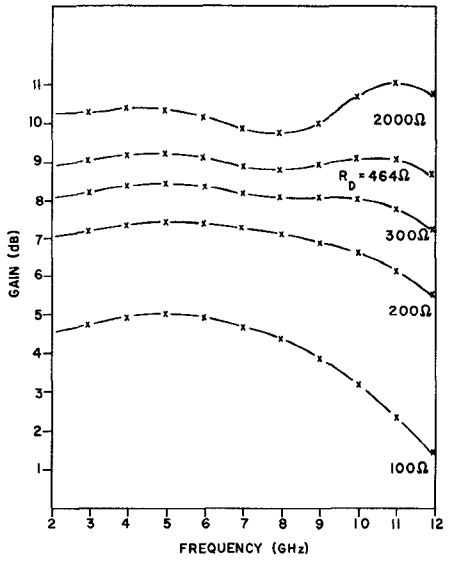

Fig. 7. Effect of drain loadings on gain versus frequency response.

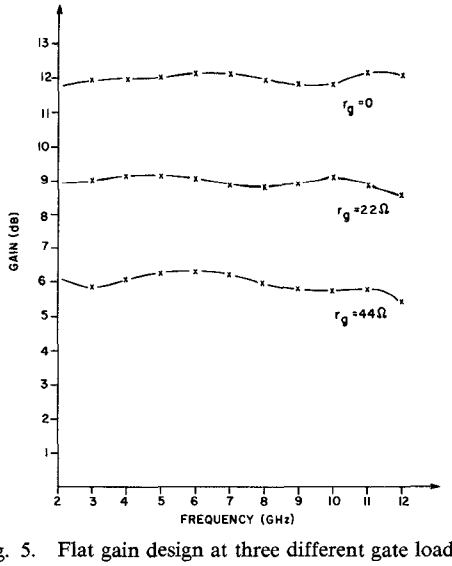

Fig. 5. Flat gain design at three different gate loadings.

gate terminals is shown in Fig. 6 for the four-cell 9-dB gain design. The decrease of the signal level at the actual gates is less than one would calculate from the $\exp(-\alpha_g l_g n)$ expression obtained on the basis of a single propagating wave in a continuous-line model. In such an approximation, reflections from the gate and drain-line impedances are not taken into account. For this reason, gain formulas (4) and (5) tend to underestimate the actual achievable gains by 1–2 dB.

In Fig. 7, the effect of the resistive drain loading on the performance of the four-cell design is examined. As the drain resistance is increased to values much larger than the 464 Ω used in the design, gain increases by about 1 dB. Note that, compared with the effect of gate loading, the effect of the drain loading is smaller. As the loading is increased further by decreasing R_D, gain at first comes down uniformly, then faster at the high band end. Since the attenuation constant α_d is independent of frequency to first order, this behavior indicates that FET's first in line

contribute to the high-frequency performance more than the later stages. This is not surprising when we consider that the later FET stages are not excited as well as the first few stages at the high end of the frequency band.

III. Circuit Fabrication

Circuits are processed on vapor-phase epitaxy layers grown by the $AsCl_3$ system on semi-insulating GaAs substrates. The three layer structures consist of a high-doped contact layer ($n > 2\times10^{18}$ cm^{-3}, $t = 0.2$ μm), an active layer of moderate doping ($n = 9\times10^{16}$ cm^{-3}, $t = 0.3$, μm), and an undoped buffer region ($n < 5\times10^{13}$ cm^{-3}, $t = 2.0$ μm). Device isolation is achieved with a combination of a shallow mesa etch and a damaging $^{16}O^{+}$ implant.

Ohmic contacts are formed by alloying the standard Ni/AuGe metalization into the surface. The ohmic metal also forms the bottom plates of the thin-film capacitors. The gates, which are recessed, consist of a Ti/Pt/Au (1000/1000/3000 Å) metalization and are nominally 1 μm long.

The capacitor dielectric is a plasma-assisted CVD silicon nitride layer with a nominal thickness of 5000 Å and relative dielectric constant of 6.8. The thin-film resistor material is titanium. During deposition, the film thickness is monitored using a four-point resistance setup to assure a final sheet resistance of about 6.7 Ω/□.

The final frontside processing steps define the transmission-line structures, capacitor top plates, and air-bridge interconnects. All of these are fabricated out of plated gold about 3–4 μm thick. The air-bridges are used to connect from the GaAs surface to the top plates of the MIM capacitors without having to cross the dielectric step and risk shorting of the structure.

After plating, the wafer is lapped to its final thickness of 100 μm by first mounting it upside down on an alumina substrate. Via-holes are etched through the wafer to ground points on the frontside. The via-holes are aligned by looking through the slice with infrared optics to see the frontside pattern. Finally, a chip-dicing grid is defined in the back by alignment to the via-hole pattern and the region between the grid lines (the chip back) is plated to a thickness of 12–15 μm with gold. The grid lines are etched through the frontside, the wafer dismounted, and the chips allowed to simply fall apart.

IV. Circuit Description and Experimental Results

The circuit shown in Fig. 1 is realized in monolithic form on 0.1-mm GaAs with 50-Ω input and output lines, as shown in Fig. 8. The chip dimensions are 2.5 mm×1.65 mm. The total gate periphery is 4×300 μm with nominal 1-μm gate length. Devices typically have −2-V pinchoff voltages. The design calls for 9-dB gain in the 2–12-GHz frequency band. The experimental performance in the 0.5–14-GHz frequency band is shown in Figs. 9 and 10. In Fig. 10, the predicted gain points are also included, indicating good agreement with the 9-dB±1-dB experimental gain performance obtained in the 2–13-GHz band. The input–

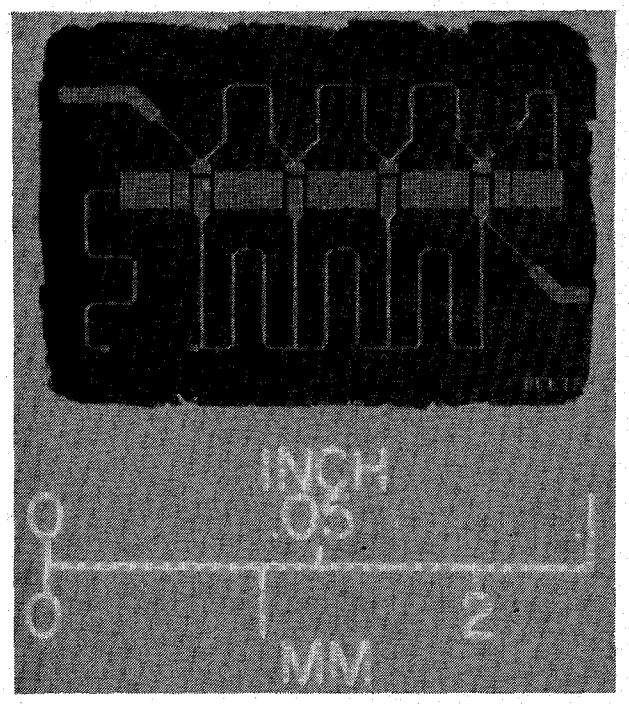

Fig. 8. GaAs monolithic traveling-wave amplifier chip.

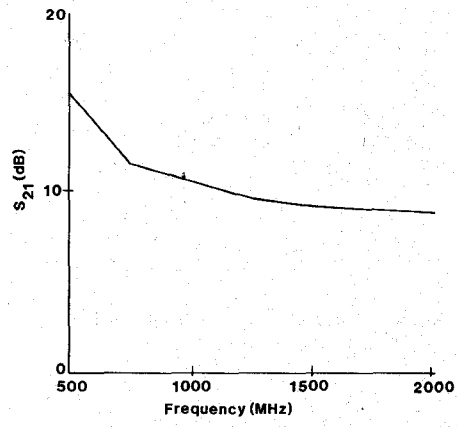

Fig. 9. Experimental performance of monolithic traveling-wave amplifier at 0.5–2-GHz frequency range.

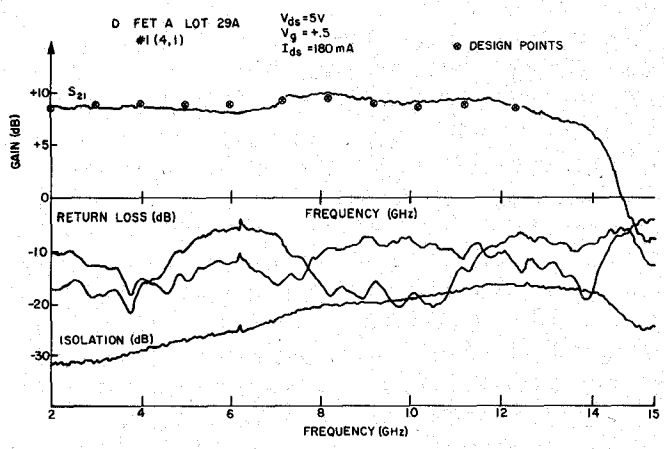

Fig. 10. Experimental performance of monolithic traveling-wave amplifier at 2–14-GHz frequency range.

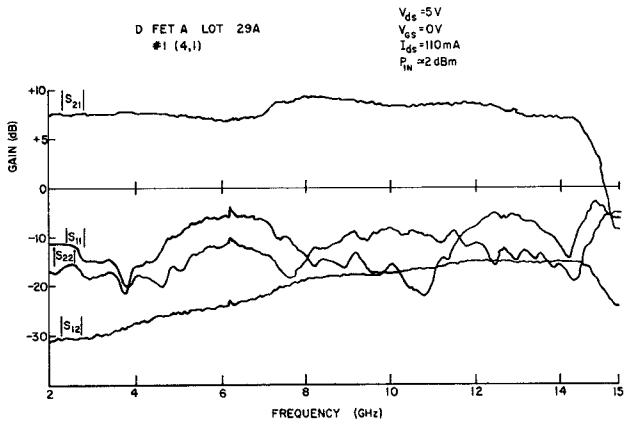

Fig. 11. Experimental performance of the traveling-wave amplifier at zero gate bias. Note the increase in bandwidth up to 14.5 GHz.

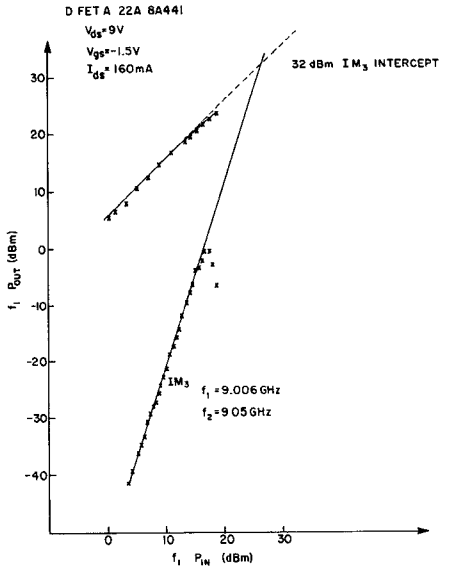

Fig. 12. Third-order intermodulation measurement results for an amplifier with −4-V pinchoff devices.

output isolation is better than 18 dB across the band. In Fig. 11, performance at 0-V gate bias is shown. The gain is 1-dB lower at 8 dB±1 dB, but the high-frequency end of the gain curve now extends to 14.5 GHz, in agreement with (6).

To observe the power performance, circuits with 4-V pinchoff voltages were processed. These circuits gave power outputs of 300 mW at the 1-dB gain compression point with 6-dB gain and 17 percent power added efficiency at 10 GHz. In Fig. 12, the results of third-order intermodulation measurements are presented.

The measured noise figure of the amplifier when the FET's are biased at the minimum noise condition is 3.9 dB at 4 GHz and 5.4 dB at 10 GHz with 5.4-dB associated gain. We have also developed a computer program which can predict the noise performance of a traveling-wave amplifier. Fig. 13 shows a typical amplifier configuration with the associated noise generators. In this figure, e_j and i_j with $j=1$ to 4 represent the intrinsic FET noise generators, all referred to the gate side; e_g and e_d represent the noise

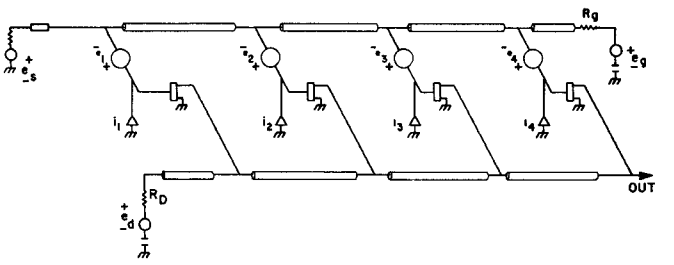

Fig. 13. Schematic representation of the relevant noise sources in a four-cell traveling-wave amplifier.

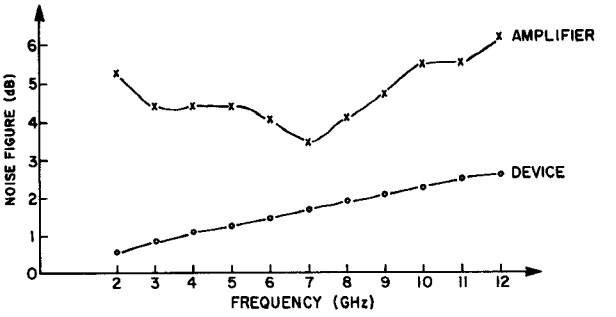

Fig. 14. Calculated noise performance of the amplifier in comparison to the noise performance of the devices used.

generated by the gate- and drain-line load resistances, respectively. Given the noise parameters R_n, Y_{opt}, and F_{min} of the FET's used in the circuit, the program calculates the contribution of all the individual noise generators to the overall noise figure of the amplifier, including the correlations between e_j's and i_j's. We have applied the program to a 2–12-GHz amplifier design using the low-noise S-parameters of 300-μm periphery devices. The noise performance of such an amplifier with an associated gain of 5.5 dB is shown in Fig. 14.

V. Conclusion

We have described a traveling-wave amplifier with 9-dB ±1-dB gain over a 1–13-GHz bandwidth, demonstrating that traveling-wave amplification in microwave frequencies is realizable with GaAs FET's and distributed input and output lines. The experimental results are in excellent agreement with the theoretical predictions. The complete amplifier is realized with monolithic circuit technology on a 2.5-mm×1.65-mm×0.1-mm chip.

We have examined the microwave performance of such a structure as a function of the important FET and amplifier parameters, derived gain expressions including the effect of gate- and drain-line loading, and given initial results on the noise performance of such a structure.

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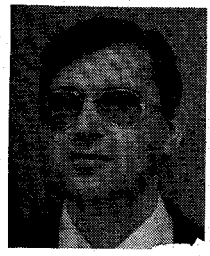
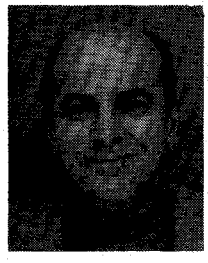


Yalcin Ayasli (M'79) was born in Ankara, Turkey, on February 14, 1946. He received the B. S. degree in electrical engineering from Middle East Technical University, Ankara, Turkey, in 1968. He received the M.S.E.E. and Sc.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, in 1970 and 1973, respectively.

From 1973 to 1979 he was a faculty member in the Middle East Technical University, Electrical Engineering Department, where he has been engaged in research and development of wide-band stripline circulators and active microwave circuits. In 1979 he joined the Raytheon Research Division, Waltham, MA, on leave from the Middle East Technical University. His present research activities involve design and evaluation of various microwave monolithic integrated circuits.



Robert L. Mozzi received the B.S. and M.S. degrees in physics from Villanova College in 1953 and the University of Pittsburgh in 1955, respectively. Following employment as an Analytical Physicist at Pratt and Whitney Aircraft, he has been a member of the Raytheon Research Division since 1957 and received a Ph.D. in physics from the Massachusetts Institute of Technology in 1968 after completing studies there under a Raytheon advanced study grant program. His earlier work was in X-ray diffraction and he has published several papers on methods for its application to the study of solids and on determinations of the structures of crystalline and amorphous materials, most notably vitreous silica and boron oxide.

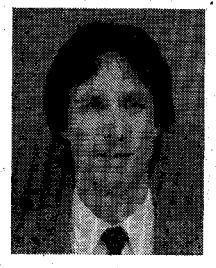
Since graduating from MIT he has been responsible for establishment of an ion implantation facility and research program at the Research Division, and more recently his major interest has been exploring new technologies for the fabrication of GaAs FET's and monolithic circuits with particular emphasis on ion implantation and on high resolution optical and electron beam lithography.

Dr. Mozzi is a member of the American Physical Society.

James L. Vorhaus was born in St. Louis, MO, on August 2, 1950. He received the B.S. degree (with highest honors) in engineering physics from Lehigh University, Bethlehem, PA, in 1972, and the M.S. and Ph.D. degrees in physics from the University of Illinois, Urbana–Champaign, IL, in 1974 and 1976, respectively.

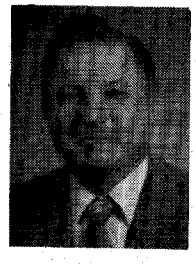
While at the University of Illinois he did research on the thermal transport properties of copper alloys at low temperatures. In 1976 he joined the Research Division of the Raytheon Company, Waltham, MA, where his initial work involved the development of GaAs FET process technology and the design of, and applications for, dual-gate GaAs FET's. His current work is focused on the design, fabrication, and testing of monolithic microwave GaAs IC's.

Dr. Vorhaus is a member of Phi Beta Kappa, Tau Beta Pi, and the American Physical Society.



Leonard D. Reynolds, Jr., was born in Kingstree, SC, in 1953. He received the B.S.E.E. and M.S.E.E. degrees from Clemson University, Clemson, SC, in 1975 and 1978, respectively.

He joined the Special Microwave Devices Operation at Raytheon in 1978 to work on GaAs FET characterization. Since 1980 he has worked in development of GaAs MMIC's at Raytheon's Research Division.



Robert A. Pucel (S'48-A'52-M'56-SM'64-F'79) received the B.S. and M.S. degrees in 1951 and the D.Sc. degree in 1955, in electrical communications, all from MIT, Cambridge, MA. From 1948 to 1951 he was a Test Engineer on the MIT Cooperative Course with General Electric Company.

Following his graduation, he joined the Microwave Tube Group at the Research Division of Raytheon Company. A year later he returned to MIT where from 1952 to 1955 he was a Staff Member of the MIT Research Laboratory of Electronics doing theoretical studies in time-domain network synthesis. Both his master's and doctoral dissertations were in the field of network synthesis. In 1955 he rejoined the Research Division of Raytheon. From 1965 to 1970 he was Project Manager of the Microwave Semiconductor Devices and Integrated Circuits Program. From 1970 to 1973 he served as a Consultant to the Microwave Transistor Group of the Power Tube Division. Presently he is a Consulting Scientist at the Research Division. His work has involved both theoretical and experimental studies of most microwave semiconductor devices, including their signal and noise properties. His activities have also included studies of microstrip propagation on dielectric and magnetic substrates as well as research on miniature dielectric cavities. His most recent work is in the field of FET oscillator noise studies and monolithic GaAs analog circuits. He has published extensively on most of these topics.

Dr. Pucel is a co-recipient of the 1976 Microwave Prize granted by the MTT Society of the IEEE. He also has been elected the National Lecturer for the Microwave Theory and Technique Society for 1980–1981. He is also a Registered Professional Engineer of the Commonwealth of Massachusetts.